The ATLAS hadronic calorimeter at the LHC and the phase II upgrade program

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29.6.2015

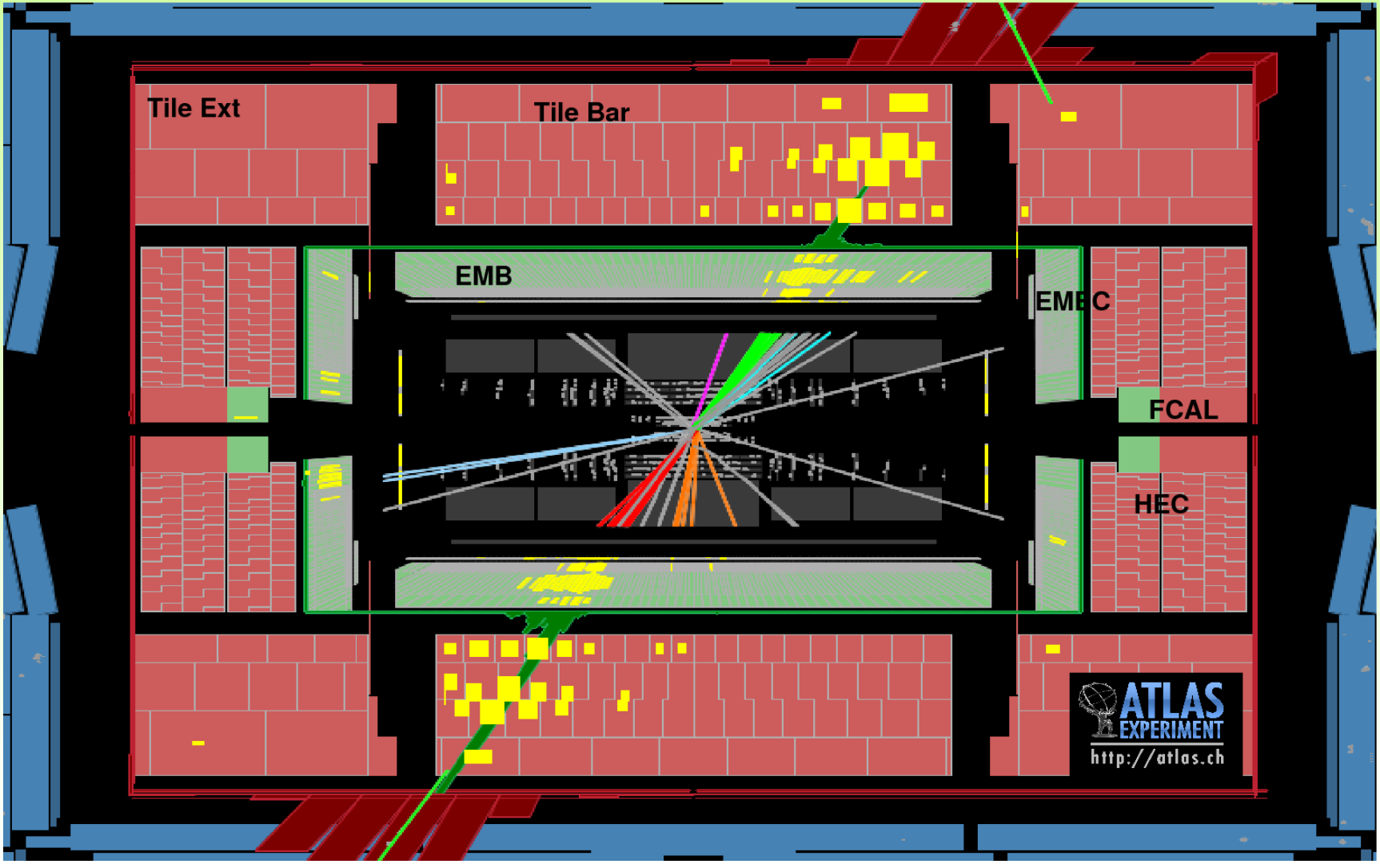
on behalf of the ATLAS Tile Calorimeter System

Overview

- Hadronic calorimeter in ATLAS
- Upgrades
- Summary

Hadronic calorimeters

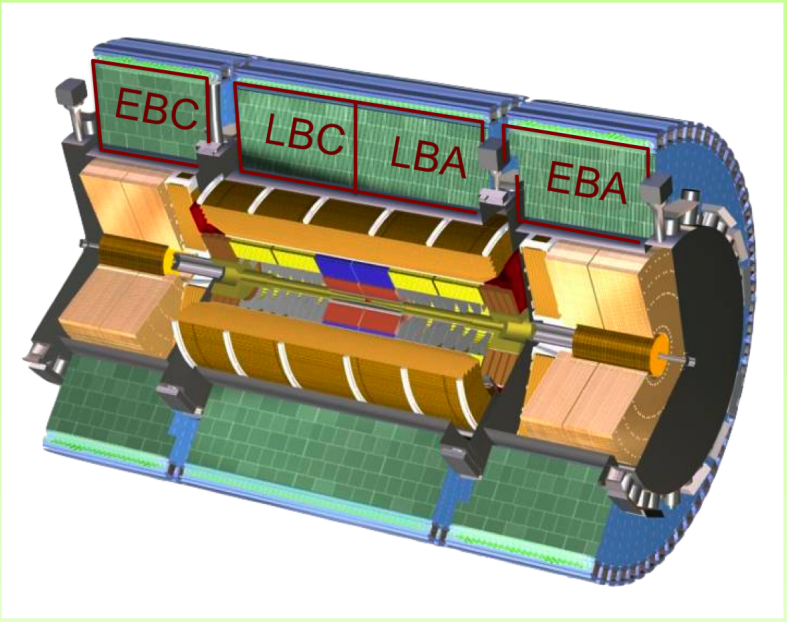
- Tile calorimeter - TileCal
- Liquid argon hadronic end-cap - LAr HEC



TileCal

Measurement of the energy of hadrons and jets and reconstruction of E_T^{miss}

- Energy resolution for jets: $\sigma/E = 50\%/\sqrt{E} \oplus 3\%$
- Linear within 2% (up to 4 TeV jets)

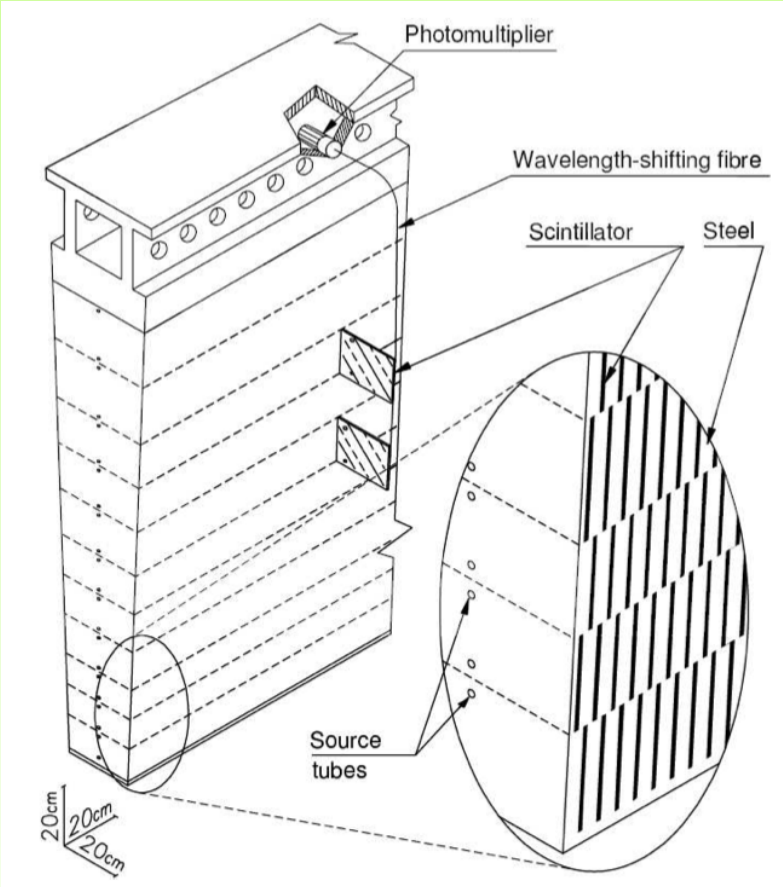


- Four partitions - EBC, LBC, LBA, EBA
- Each partition is composed of 64 modules
- Each LB module is composed of 45 cells

TileCal

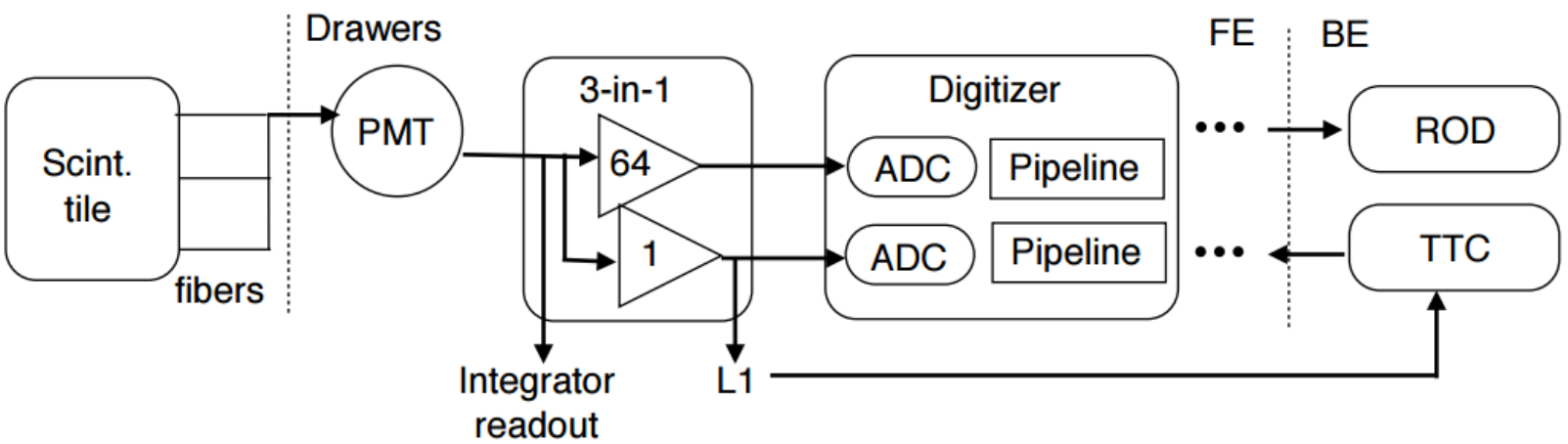
Design

- TileCal is made of plastic scintillators and steel as an absorber
- Light produced in scintillators is transmitted by wavelength shifters to photomultiplier tubes (PMTs)
- Each cell is read-out by two PMTs to achieve uniform response
- Signals from the PMTs are processed by the on-detector electronics



Readout

- Signals from several tiles are collected by wavelength shifting fibers and sent to PMTs
- The signal of each PMT is read by one electronic channel
- PMT analog signal $\rightarrow$ 3-in-1 for shaping and amplification (bi-gain 1:64), slow integrator readout, and analog signal to L1 trigger
- Dynamic range of ADC: $\sim$10 MeV to 800 GeV
- Two channels (collecting light from either side of tile) $\rightarrow$ readout one cell



Energy calibration

- Channel energy reconstructed using Optimal Filtering algorithm: $A = \sum_{i=1}^{n=7} a_i S_i$
- Weights a_i derived using known pulse shape and sample noise autocorrelation matrix
- Initial exposure to test beam of electrons and muons used to set overall electromagnetic scale (pC$\rightarrow$ GeV)
- Cesium: calibration of scintillator tiles and PMTs (read out by integrator circuit)
- Laser: calibration of PMTs and readout electronics
- Charge injection system (CIS): injection of known charge into front end electronics, calibration of readout electronics (ADC$\rightarrow$ pC)
- $E_{chan} = A \cdot C_{pC \rightarrow GeV} \cdot C_{Cs} \cdot C_{las} \cdot C_{CIS}$

Cesium and charge injection system calibration

Cesium calibration

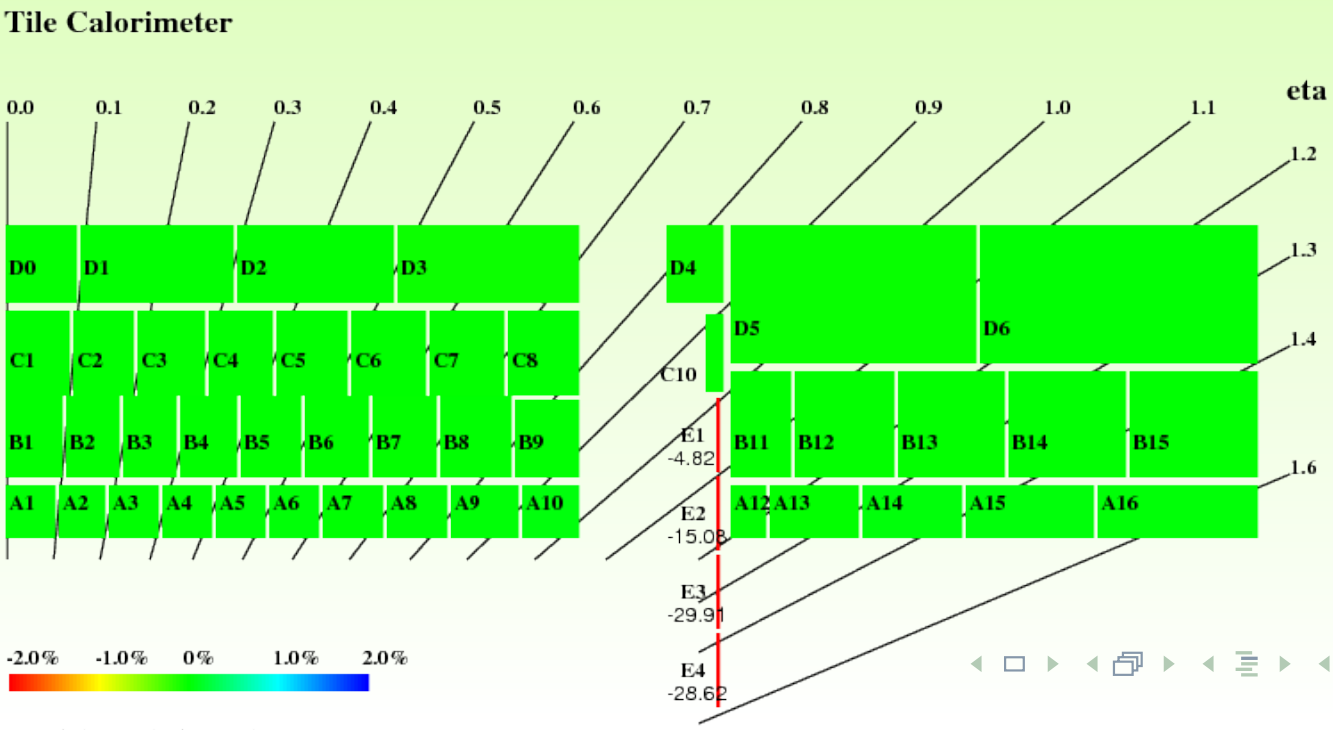
- ^{137}Cs used to calibrate scintillator tiles by emitting 0.662 MeV photons:
- 3 movable Cs sources located in closed circuit system
- Cs sources are moved through every tile by hydraulic system
- Maintain the overall energy calibration
- Apply calibration corrections for residual cell differences (cell inter-calibration)

Charge injection system - CIS

- Injection of known charge into 3-in-1 cards to measure electronics response (pC$\rightarrow$ADC)
- For high gain and low gain
- Correction for non-linearities
- CIS calibration $\sim$ 2/week

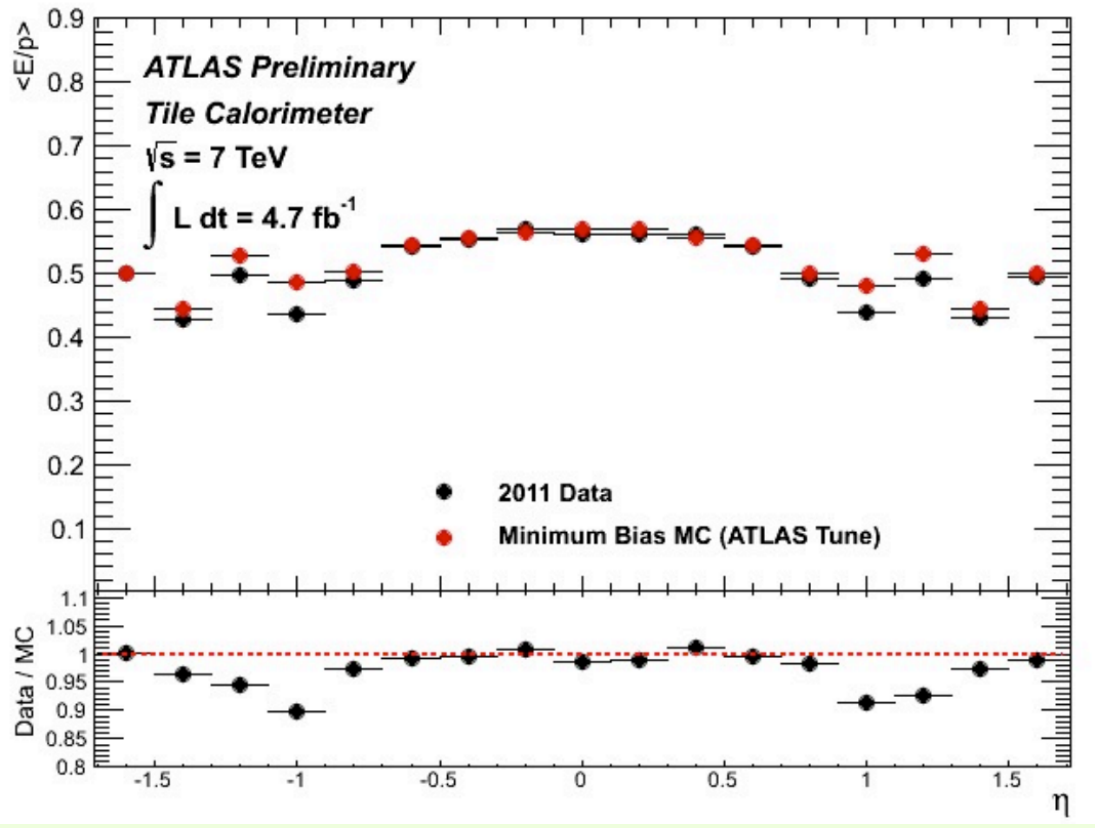
Laser calibration

- Pulse of laser light sent to PMTs
- Monitor and measure individual PMT gain variation between Cs scans
- Monitor time of individual channels
- Laser calibration runs 2/week, and laser pulses sent during empty bunch crossings



Performance during Run 1

- Tile DQ efficiency for p-p collisions: 2012 was 99.6% (2011: 99.2%, 2010: 100%)
- Performance with hadrons(study isolated charged particles that shower in TileCal): measure momentum (p) from inner detector, and compare with energy of shower in calorimeter (E) from clustering around track projection $\rightarrow$ response given by E/p

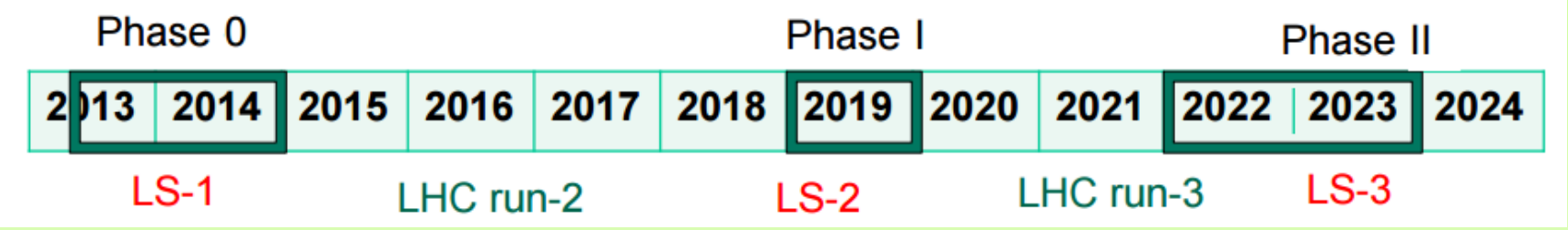


- data and MC agree within 3% (except at LB and EB transition regions $0.8 < |\Delta| < 1.1$, deviation up to 10%)

Motivation for upgrades

- Better radiation tolerance
- Ageing of components(>10 years) $\rightarrow$ reached the end of components designed lifetime
- Simplify and reduce maintenance needs
- Increased luminosity demands for a better precision and finer granularity in the trigger. One major concern with the increased luminosity is the effect of pile-up (consecutive interactions in the same cell, pulses piling up)
- Improve the reliability
- LHC upgrade in 2023 aim for a luminosity of $(5-10) \times 10^{34} cm^{-2} s^{-1}$
- More events accepted with current criteria
- More data generated $\sim x500$

Upgrade timeline

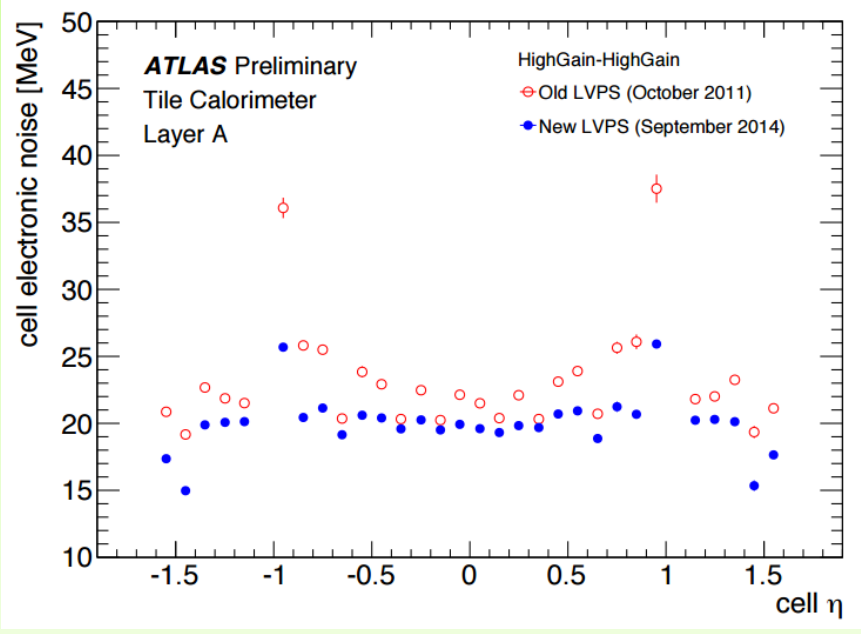


- Phase 0 2013-2014: install new LVPS, maintenance of front-end (FE) boards, Tile 3rd layer in the Muon Trigger logic for $1.3 < |\Delta| < 1.5$
- Phase I 2019: replacement of gap scintillators
- Phase II 2022-2023: complete upgrade of the FE and back-end (BE) electronics for High Luminosity LHC (HL-LHC) - details presented on next slides

Phase 0

Low Voltage Power Supplies

- Replaced all LVPS by newer versions
- Number of LVPS trips significantly reduced
- Less corrupted data that resulted from LVPS trips
- Improved noise: lower electronic noise

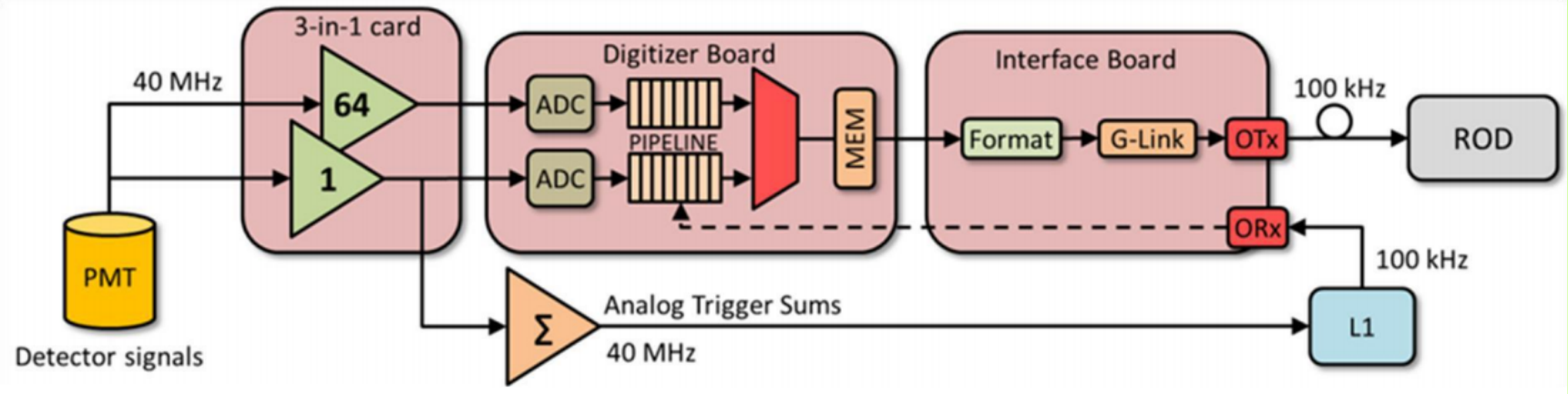


Phase 0

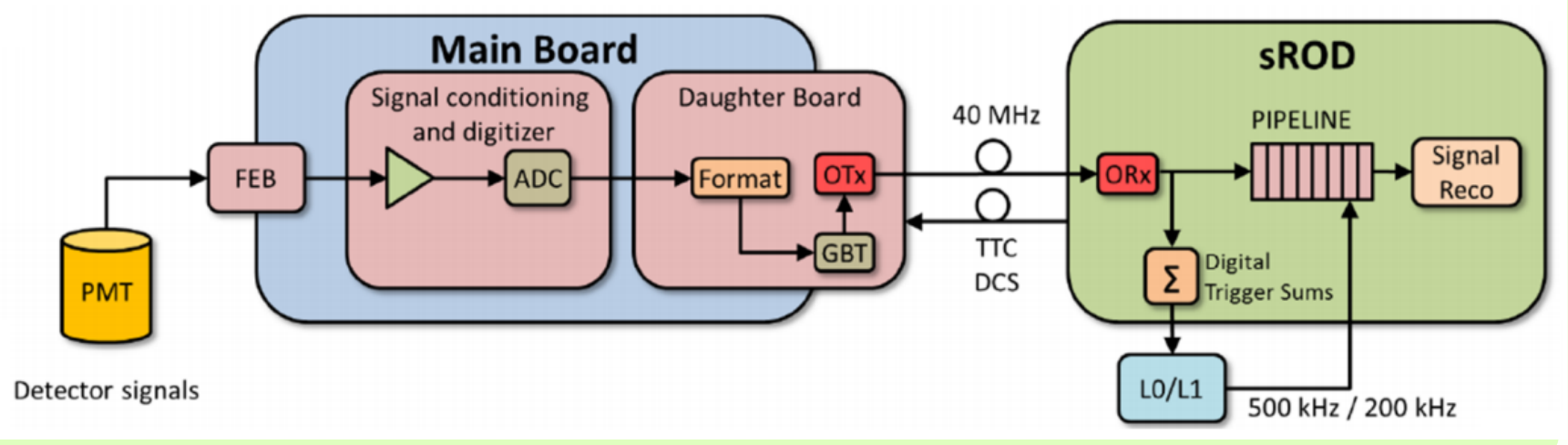
- Open, inspect and repair FE electronics in all modules
- Run full calibration (pedestal, charge injection, laser system) 3x per week
- Updated of Cesium system hydraulics
- Updated the laser system to improve the light mixing to avoid non-uniformities in light distribution $\rightarrow$ more precise constants
- Modified front-end electronics for E1-E4 cells to adjust dynamic range
- Installed previously missing 8 (of 64) E3 and 8 (of 64) E4 counters per EB absent in Run 1 (due to MBTS readout)

Phase II

Current read-out architecture



Phase II architecture



Phase II read-out architecture

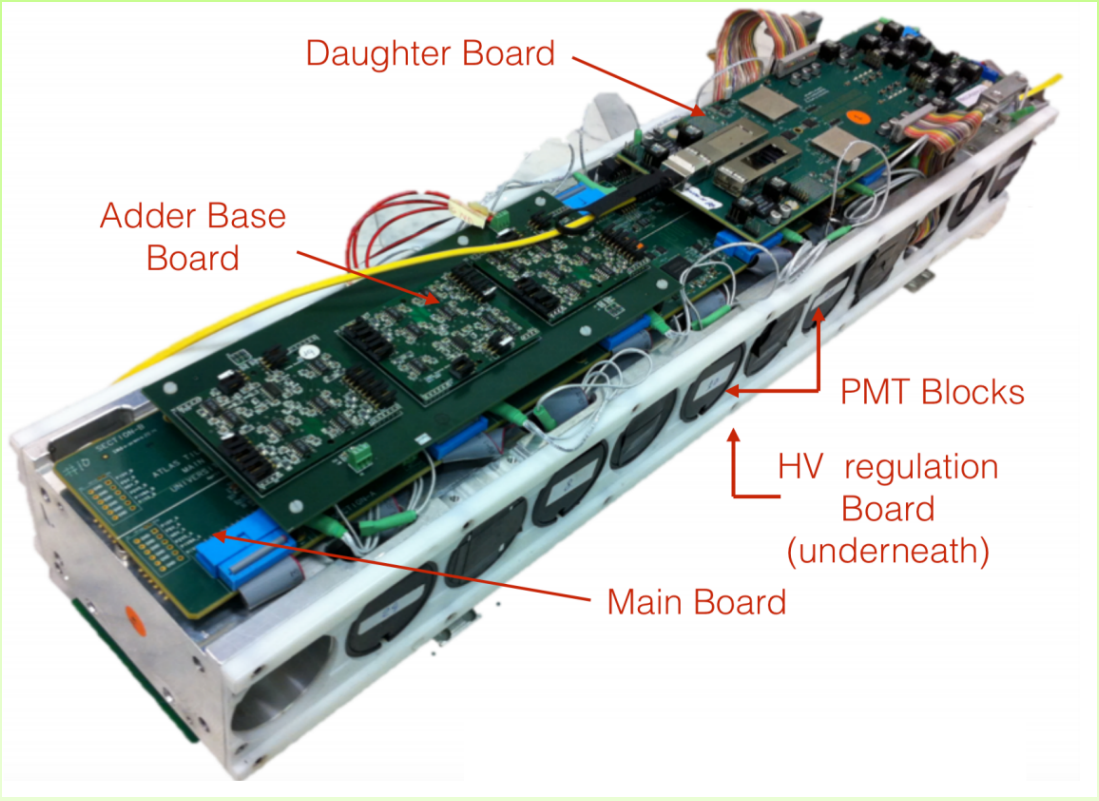
- Present sys.: Analog output with reduced granularity for L1 trigger. The digital output is at 100 kHz. The events are pre-selected by the Level-1 trigger sys. from 40 MHz to 100 kHz.
- New system: output of digital data at 40 MHz. The hardware-based triggers, L0/L1 , will use digital data. Full granularity will be used.
- Simplification: reduced number of boards and less inter-connections
- FE board: three options available
- Main board: PMT signal conditioning and digitization

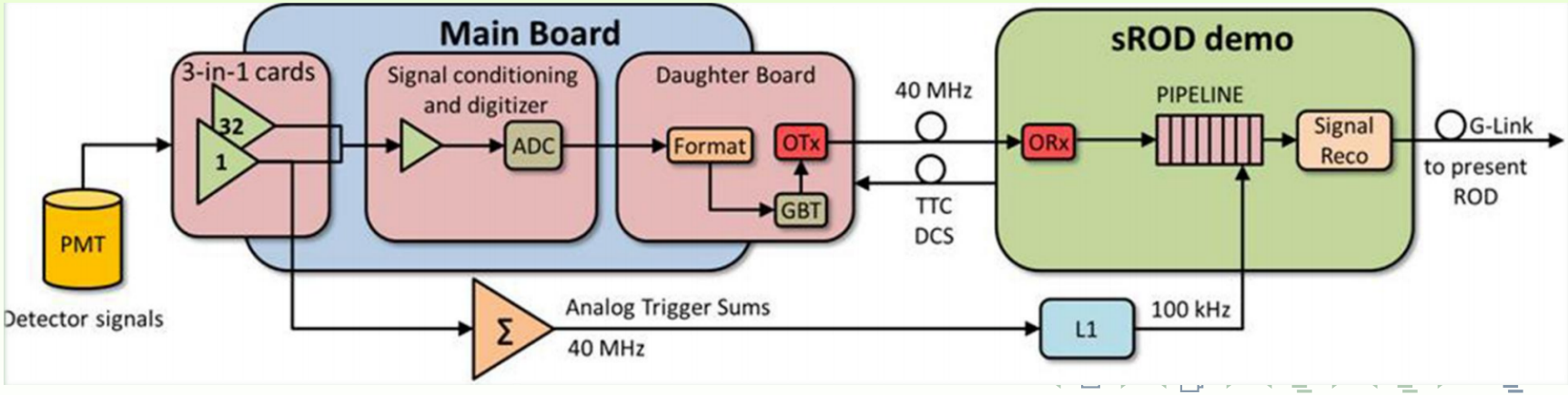
Phase II read-out architecture

- Daughter board: high speed optical communication for transmission of full data at 40 Mb/s to sROD
- Super-ROD (sROD): pipelines and de-randomizers. Data information for the LVL0/LVL1 trigger system.
- More modular: 1 superdrawer splits in 4 independent mini-drawers. One LB module served by 8 mini-drawers. + largely enhanced redundancy of the RO: no single points of failure.

Tile Demonstrator

- Evaluation of the design and technology
- Similar as possible to Phase-II system while backward compatible with the present system
- Planned insertion in Tile Calorimeter in 2015-2016





Front-end board options

- Modified 3-in-1 FE board
- The QIE front-end board (Application-Specifc Integrated Circuit ASIC)
- FATALIC 4 front-end board (ASIC)
- Only one will be choosen

Front-end board options

- Modifed 3-in-1 Board
- Based on the current design
- Improvements in radiation hardness, linearity and noise
- Receives signal from a PMT to shape and amplify it
- 17-bit dynamic range

- QIE FE board
- Uses a Charge Integrator and Encode (QIE) chip
- Splits the current into 4 different ranges with no shaping.
- Useful for pile-up - can operate every 25 ns (40 MHz)
- 17-bit dynamic range

- FATALIC FE board
- Combines two ASIC solutions (TACTIC and FATALIC).
- FATALIC - Front-end for Atlas TilecAL Inegrated Circuit
- TACTIC - Twelve bits AdC for atlas Tilecal Integrated Circuit
- Shaping with three different ranges (1, 8, 64)
- 12-bit pipelined ADC
- Can operate every 25 ns (40 MHz)

Mainboard and daughter board

Mainboard

- MB-1 (Modified 3-in-1)
  - Digital control of 3-in-1 with 4 FPGAs
  - Digitization and transmission to DB via FMC connector
  - Redundant design (all levels)
- MB-2 and MB-3 (QIE & FATALIC)
  - Different from MB-1, since they use different FE boards
  - No ADCs needed

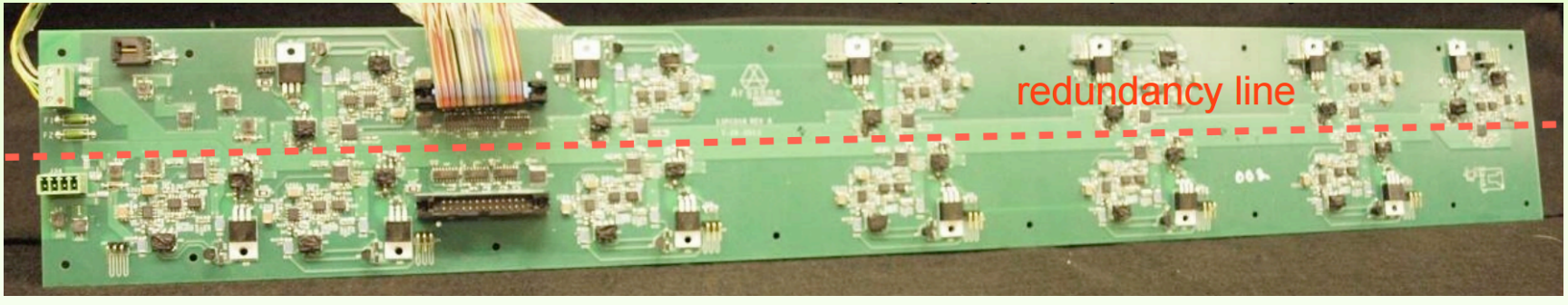
Daughter board

- High speed communication with back-end electronics
- Formats and transmits read out and DCS data
- Receives configuration and control commands from DCS
- Configurable via optical link - Complete 4-fold redundancy

HV board

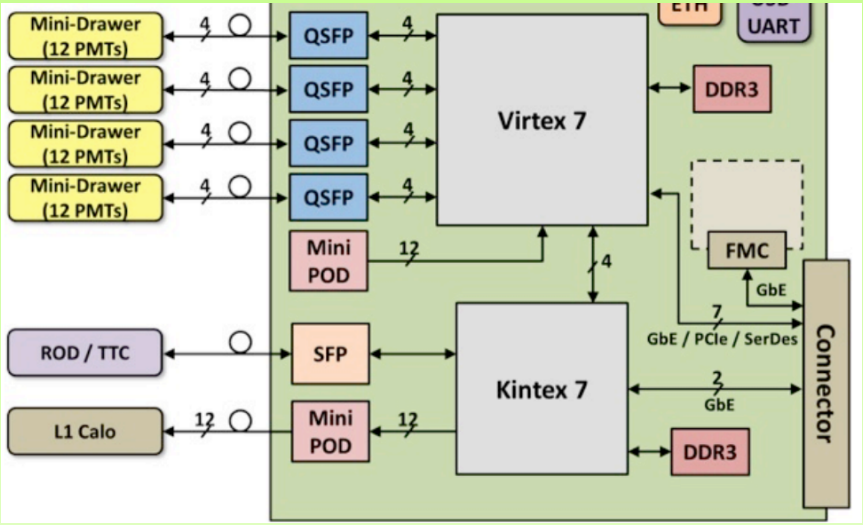
Two options available - Local or Remote

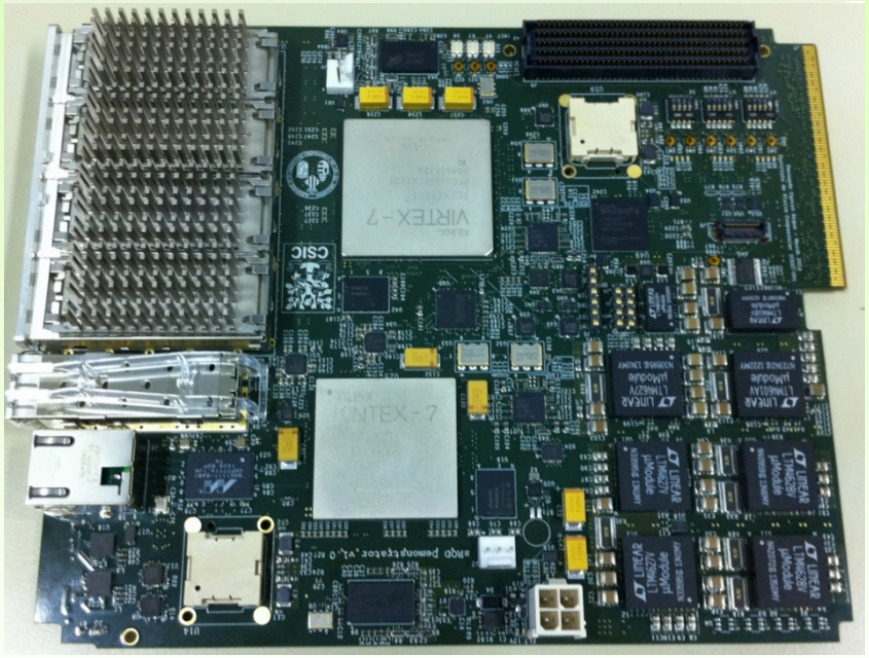
- Local (HVOpto) largely based on the existing system use Kintex-7 FPGA in the daughter board for control of HV settings and monitoring
- Introduce possibility of switching on/off individual PMTs
- Remote (HVRem) the existing local regulation system is moved to USA15 and individual cables are routed to the PMTs. First prototype built, under investigation for Phase-II.



sROD demonstrator

- sROD interfaces the FE with current ROD and DCS - Completely digital means better resolution
- Main data read out
- Trigger and Timing Control distribution
- DCS commands to front-end
- Read-out of a complete super-drawer (4 mini-drawers)
- Designed for new back end infrastructure
- Status: first prototype received, testing ongoing.





Summary

- Performance of the Tile hadronic calorimeter in Run 1 (2009-2012) was great (data quality efficiency $\sim$99.6%)
- During LS1 were opened, inspected and repaired front-end electronics in all modules + updated calibration systems
- Upgrade of Tile Calorimeter for HL-LHC is progressing well
- Complete redesign of the front and back end electronics - few alternative choices need to be fully evaluated under beam tests.
- Early insertion scheduled for 2015/2016 in next detector opening
- Test beams begin 2015 to 2016