The ATLAS hadronic calorimeter at the LHC and the phase II upgrade program

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The Tile Calorimeter of the ATLAS experiment at the Large Hadron Collider (LHC) is the central hadronic calorimeter designed for energy reconstruction of hadrons, jets, tau-particles and missing transverse momentum. The LHC is scheduled to undergo a major upgrade for the High Luminosity LHC (HL-LHC) in 2024-2026. The ATLAS upgrade program for high luminosity is split into three phases. Phase-0 occurred during 2013 - 2014 and prepared ATLAS for the LHC Run 2. Phase-I, scheduled for 2019-2020, will prepare ATLAS for the LHC Run 3 and Phase-II, which is scheduled for 2024-2026, will prepare ATLAS for the HL-LHC.

1 Hadronic Calorimeter in ATLAS

1.1 TileCal Electronics

The ATLAS Tile calorimeter (TileCal) [1] is the central hadronic calorimeter of ATLAS. TileCal is a sampling calorimeter composed of plastic scintillating plates as active medium and steel plates as absorber. It is divided in a central barrel (divided in 2 partitions - LBA, LBC) and two extended barrels (EBA, EBC) (see Fig. 1). Each cylinder is composed of 64 modules.

The interaction of high energy particles with the steel creates showers of lower energy particles, which produce light in the scintilators. The light is transmitted through wavelength shifting (WLS) fibers to photomultipliers (PMTs). Adjacent tiles and their WLS fibers are grouped together to form TileCal cells. For each cell the fibers are read-out from two sides by two PMTs. Thus, each cell is read out via two different electrical signal paths. The central barrel modules are divided into 45 cells each, while the extended barrels modules are divided into 14 cells. The analog signal from the PMT is processed by the 3-in-1 card (Front-End Board), which is responsible for signal conditioning and amplification providing three analog signals as outputs, two for the detector readout (low and high gain, with a gain ratio of 1:64.) and another for triggering purposes. The signals from either low-gain (LG) or high-gain (HG) channel are simultaneously digitized with a 10-bit ADC in a rate of 40MHz and stored in the front-end pipeline memory. The TileCal front-end (FE) electronics is located inside the outermost part of the modules.

The main component of the back-end (BE) electronics is the Read-Out Driver (ROD). The ROD performs preprocessing and gathers data coming from the front-end electronics at a maximum level 1 trigger rate of 100 kHz. The digitized signals are reconstructed with the Optimal Filtering algorithm. This algorithm computes the signal amplitude, time and quality factor for each channel at the required high rate (up to 100 kHz). The ROD sends data to the Read-Out Buffers (ROB) in the level 2 trigger. The TileCal level 1 trigger signal is produced by analog summation of up to six signals on the Trigger Board. The level 1 trigger has to reduce the event rate from 40 MHz to 100 kHz.

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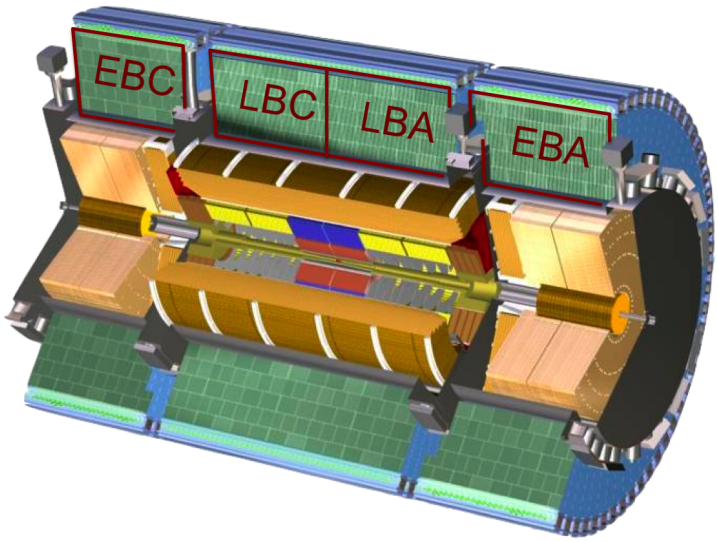

Figure 1: A picture of the ATLAS detector displaying layout of calorimeters. The TileCal barrels are at the outer side marked as EBC, LBC, LBA, EBA. Between the TileCal and beam pipe are trackers and Liquid Argon (LAr) calorimeter. The LAr calorimeter includes electromagnetic (EM) calorimeter in the central area (LAr EM barrel, corresponding to the LBC, LBA) and combination of the EM and hadronic calorimeter (LAr EM end-cap and LAR hadronic end-cap, corresponding to the area between extended barrels of TileCal and beam pipe).

1.2 The Calibration of the TileCal

The energy deposited in the TileCal cells is measured in ADC counts, but it needs to be converted into GeV following the equation:

$$E[\mathrm{GeV}] = \mathrm{A} \times \mathrm{C_{pC\to GeV}} \times \mathrm{C_{Cs}} \times \mathrm{C_{las}} \times \mathrm{C_{CIS}} \tag{1}$$

where A is the measured channel signal amplitude.

$C_{pC\to GeV}$ is a constant to convert the charge to the electromagnetic scale (measured during test beam using electrons and muons).

The injection of known charge from the charge injection system (CIS) into front end electronics determines calibration of readout electronics C_{CIS}.

The Cesium system is a movable radioactive source circulated through all the detector cells to equalize their response. The signal generated by the Cs source is read out through a special electronics that integrates the analog PMT signals. The Cs system determines C_{Cs} constant.

The laser system main purpose is to monitor the photomultipliers tubes and determines the C_{las}.

2 Upgrade Program

The main goals of the TileCal Phase-II upgrade are the replacement of the aging electronics, the increase of radiation tolerance, the improvement of system reliability, to simplify and reduce maintenance needs, to increase data precision and finer granularity in the trigger. One major concern with the increased luminosity is the effect of pile-up (consecutive interactions that contribute to signal in the same cell, pulses piling up).

2.1 Phase-0 Activities

Frequent trips of the low voltage power supply (LVPS) were a common problem during Run 1. To solve this problem all LVPS have been replaced by the newer versions in the Long Shutdown 1 (LS1) of the ATLAS upgrade program. Number of LVPS trips is significantly reduced, which results in less corrupted data. Significant reduction of the electronic noise is observed.

The FE electronics in all modules has been opened, inspected and repaired. The Cesium system hydraulics and laser system have been updated.

2.2 Phase-II Activities

The new read-out electronics is composed of: new FE boards (three designs are currently being developed and evaluated), new Main Boards (MB) , and new Daughter Boards (DB). Three different design options for the new FE board are under evaluation. New high voltage power supplies are also under development. A new Tile PreProcessor (TilePPr, super Read Out Driver - sROD) is being designed to replace the current ROD (see Fig. 2). A modification of the TileCal mechanics that holds the FE electronics (super-drawer) is being considered, so it will be more modular and easier to maintain. One superdrawer is divided in 4 independent mini-drawers. One LB module is served by 8 mini-drawers. This configuration will largely enhance redundancy of the read-out. Single points of failure were identified and their critical parts are duplicated in the new design. One upgraded drawer is currently tested together with a prototype of the sROD. The new Demonstrator drawer is backward compatible with the present system (see 2.6 and Fig. 4).

2.3 New Front-End Electronics for Phase II

Modified 3-in-1 FE Board

Modified Front-End Board [2] is composed of discrete components: the fast signal processing, the slow signal processing, the calibration electronics and the control bus interface.

The fast signal processing includes a passive LC shaper, two bi-gain clamping amplifiers with a gain ratio of 32 and a pair of differential drivers feeding the analog signals from the LG and the HG to the ADCs, which are located on the Main Board, for data digitization covering a dynamic range of 17 bits. The slow signal processing includes a programmable 3-gain integrator which monitors the PMT current induced by a Cs source during detector calibration and the current induced by minimum bias proton-proton interaction. The calibration electronics includes a precise charge injection circuit, integrator gain control and the control bus interface. This modified version has improved linearity and a lower noise level than the older version. The Modified 3-in-1 Card is currently equipping the Demonstrator drawer.

QIE FE Board

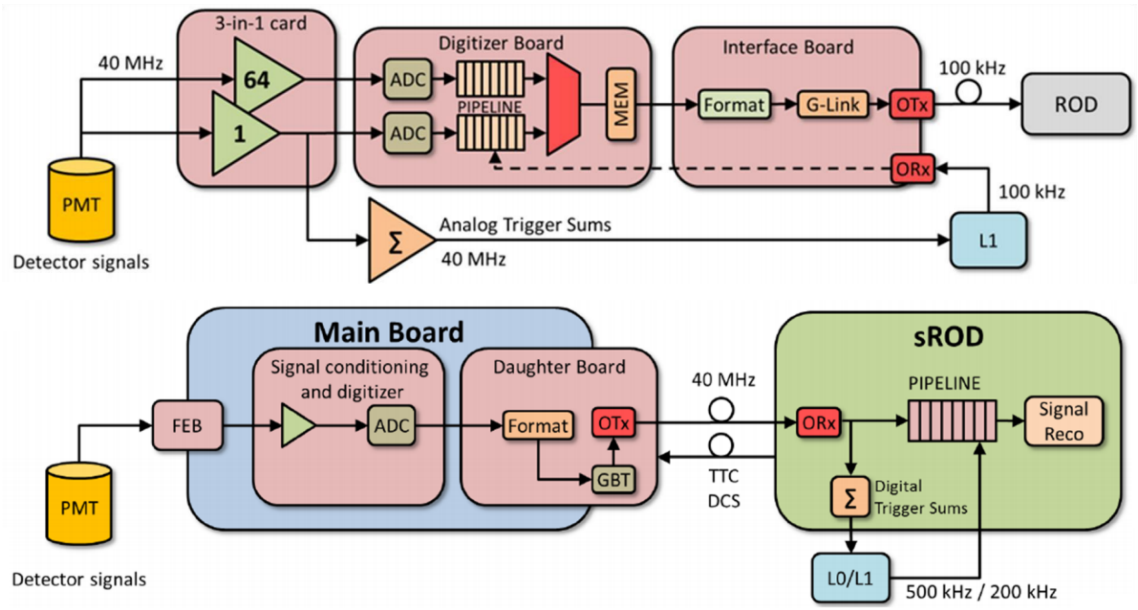

Figure 2: Current read-out structure (top) and new read-out structure (bottom).

The Charge (Q) Integrator and Encoder (QIE) chip is developed in collaboration with Fermilab and CMS HCAL. The QIE includes a current splitter providing 4 different ranges, a gated integrator and an on-board 7-bit flash ADC to cover a dynamic range of 17 bits. The QIE also includes a charge injection circuit for calibration and an integrator for source calibration. The QIE does not shape pulses. It minimizes pile up problems so it can operate every 25 ns (40 MHz).

FATALIC FE Board

Front-End for Atlas TileCal Integrated Circuit (FATALIC), includes a multi-gain current conveyor (CC) with three different gains (1, 8, 64) . The readout was using an external 12-bit pipelined ADC with a sampling rate of 40 MHz called Twelve bits ADC for ATLAS TileCal Integrated Circuit (TACTIC), but this ADC is now integrated in the most recent version of FATALIC. Moreover, FATALIC includes an integrator and a 10-bit ADC for calibration purposes. The front-end board for the FATALIC is called All-In-One Board.

2.4 Main Board and Daughter Board

The Main Board [3] is responsible for the digital control of the FEs, data organization and for the transmission of the data to the DB. The current prototype design digitizes the signals coming from Modified 3-in-1 Cards by using ADCs working at a sampling rate of 40 MHz and is used in the Demonstrator. Different MBs are developed to use QIE or FATALIC.

The Daughter Board is intended to serve as a processing board in the next TileCal electronics drawer and for high speed communication with BE electronics. The DB receives configuration and control commands from Detector Control System (DCS). The DB sends the digitized data to the super Read Out Driver (sROD) via high-speed links. The board includes complete 4-fold redundancy.

2.5 The super Read Out Driver

The sROD demonstrator is the first element of the off-detector electronics (see Fig. 3). This board is responsible for the reception and processing of the detector digital data and for the reception and distribution to the on-detector electronics of Trigger Timing and Control (TTC) signals. The sROD demonstrator also interfaces with the DCS for configuring and monitoring the on-detector electronics.

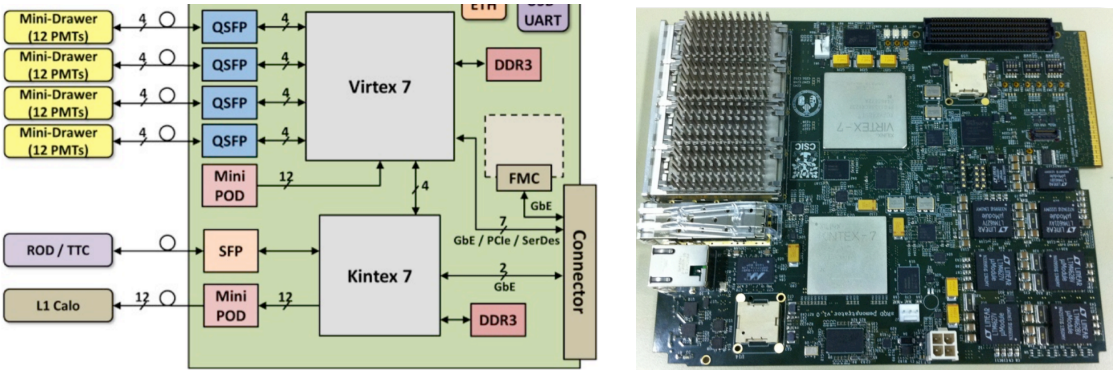

Figure 3: The super Read Out Driver.

2.6 Demonstrator

A Demonstrator project has been established in order to evaluate the design and the performance of the upgraded electronics. It should be similar as much as possible to the Phase II system while being backward compatible with the present system. Test beam campaigns are planned for 2015-2016 before the installation in the detector by the end of 2016.

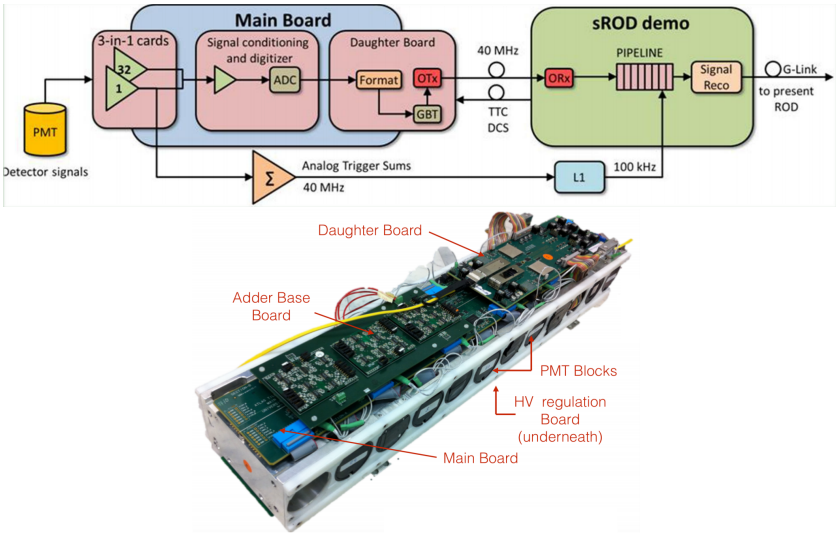

Figure 4: Demonstrator drawer.

3 Summary

The LHC is scheduled to undergo a major upgrade for the High Luminosity LHC (HL-LHC) in 2024-2026. The ATLAS upgrade program for high luminosity is split into three phases. During LS1 (Phase 0) of the LHC FE electronics in all modules of the TileCal were opened, inspected and repaired. The TileCal calibration systems were also updated. The new LVPS improved the detector reliability and reduced the electronic noise.

The Phase-II, which is scheduled for 2024-2026, will prepare ATLAS for the HL-LHC. The main goals of the TileCal Phase-II upgrade are the replacement of the aging electronics, the increase of radiation tolerance, the improvement of system reliability, to simplify and reduce maintenance needs, to increase data precision and finer granularity in the trigger.

A complete redesign of the TileCal FE and BE electronics has to be done. A few alternative choices of FE electronics, MB and DB need to be fully evaluated with beam tests by the end of 2015. One Demonstrator drawer should be installed into the TileCal by the end of 2016.

References

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[2] F. Tang, K. Anderson, G. Drake, J. Genat, M. Oreglia, J. Pilcher, and L. Price, Design of the Front-End Readout Electronics for ATLAS Tile Calorimeter at the sLHC, *Nuclear Science, IEEE Transactions on 60, 1255-1259* (2013).

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